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APPLICATION NOTE

AN10156

Sorting through the low voltage logic maze

Authors: Ramin Kowssari, Mike Magdaluyo

2002 June 06

Philips Semiconductors

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Introduction

Digital systems are running at faster speeds, operating at lower voltages, and they are becoming more highly integrated. Many functions can be integrated into FPGAs or ASICs, however, this does not mean that generic standard logic has gone away. Designers may choose to design with standard logic for the following reasons:

- The need for cheap, simple fixed functions with high speed and lower power consumption
- Space constraints requiring small packaging
- Bus driving capability
- Interfacing between mixed voltage systems
- Need for hot insertion capability
- Need for bus switching.

Today designers are challenged with the task of choosing among many low voltage logic families. This paper provides information on the various families, their key features and how to choose among them, based on the criteria listed above.

Standard Logic vs. ASICs or FPGAs

There are situations in which standard logic is more cost effective and suitable than FPGAs or ASICs. This becomes more evident when to you realize the crucial role that standard logic plays in many systems. For example, the design engineer may need to add a single function to an ASIC or FPGA in the final stage of the design due to a last minute change in the system's protocol. Rather than re-spin an ASIC or reprogram the FPGA and reinvest the engineering time, effortlessly adding a logic device that's close to the source of the problem at the critical peak of the design cycle will get the system to market on time.

Furthermore, speed, high output drive, lower power consumption, space constraints, distinctive features, and a collection of standard functions can also compel designers to utilize high-speed low voltage logic ICs. (See Tables 1 and 2).

LV/LVX	LVC/LCX	ALVC	LVT
9 ns typical t_{PD}	4 ns typical t_{PD}	2 ns typical t_{PD}	2 ns typical t_{PD}
6-8 mA I_{OH}/I_{OL}	24 mA I_{OH}/I_{OL}	24 mA I_{OH}/I_{OL}	32/64 mA I_{OH}/I_{OL}
130 ohm line drive	50 ohm line drive	50 ohm line drive	35 ohm line drive
20 µA standby current	10 µA standby current	40 µA standby current	190 µA standby current
V_{CC}: 1 - 3.6 V	V_{CC}: 1.2 - 3.6 V	V_{CC}: 1.2 - 3.6 V	V_{CC}: 2.7 - 3.6 V
Gates, MSI, bus interface functions	Gates, MSI, 8/16/32 bit bus interface functions	Gates, MSI, 8/16/32 bit bus interface functions	Gates, MSI, 8/16/32 bit bus interface functions
5 V tolerant inputs [1]	Termination resistor option	Termination resistor option	Termination resistor option
	5 V tolerant I/O	5 V tolerant inputs [2]	5 V tolerant I/O
	Supports hot swap	Bus hold feature	Supports hot swap
	Bus hold feature		Bus hold feature

Notes:
1. Vendor dependent
2. Vendor dependent
Propagation delays are approximate typicals for a '245 function

Table 1. Low voltage standard logic families and features

ALVT	AVC	AUC	CBTLV
1.5 ns typical t_{PD}	1.3 ns typical t_{PD}	1.5 ns typical t_{PD}	Sub 0.25 ns typical t_{PD}
V_{CC}: 2.3 - 3.6 V	V_{CC}: 1.2 - 3.3 V	V_{CC}: 0.8 - 2.7 V	V_{CC}: 2.3 - 3.6 V
32/64 mA I_{OH}/I_{OL}	8 mA I_{OH}/I_{OL} [1]	8 mA I_{OH}/I_{OL}	Low R_{on}, 5 ohms typical
90 µA standby current	20 µA standby current	10 µA standby current	10 µA I_{CC}
35 ohm line drive	50 ohm line drive	130 ohm line drive	Precharge circuit for hot swap
5 V tolerant I/O	Optimized for 2.5 V	Optimized for 1.8 V	Bus switches, mutiplexers, demultiplexers, exchangers
Termination resistor option	Termination resistor option	Termination resistor option	
Supports hot swap	3.3 V tolerant I/O	3.3 V tolerant inputs	
Bus hold feature	Bus hold feature	Single/dual gates, bus interface functions	
Gates,MSI,8/16/32 bit bus interface functions	Bus interface functions		

Notes:

1. 8 mA static drive, high dynamic drive to drive 50 ohm line

Table 2. Low voltage standard logic families and features

Miniature Packaging

A large growth area in packaging technology has been in gate functions in very small packages. Available in single, dual, and triple gates, IC manufacturers offer a full array of low voltage common gate functions such as OR, NOR, AND, inverters, buffers, flip-flops, multiplexers, demultiplexers, analog switches, and even bus switches. These small devices offer multiple benefits to board designers. A quick fix with a single gate is more cost effective than re-spinning an ASIC. Single and dual gates also offer space savings for space constrained boards and mobile applications and allow line layout simplification (Figure 1).

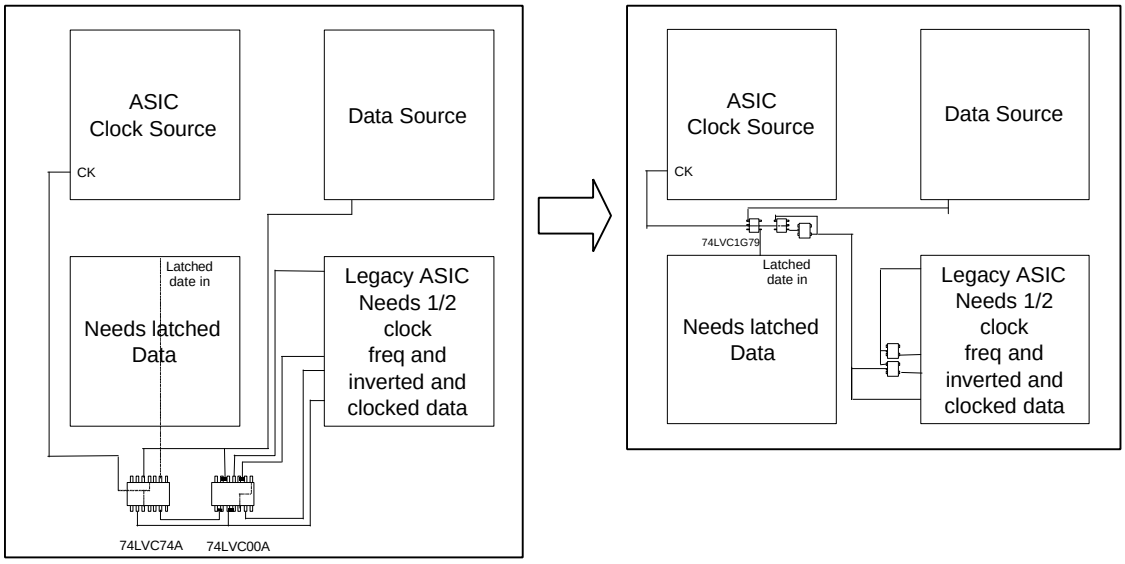

Figure 1. Example of simplified routing using single gates

As an example of space savings, the footprint of an SC70 single gate has 6 times the space savings compared to a multiple gate 14-pin TSSOP package. Several packaging options are available for single, double, and triple gates. For single and dual gates, there are 2 types of leaded 5 or 6 pin packages and 2 unleaded packages with either solder lands or solder balls shown in Figure 2:

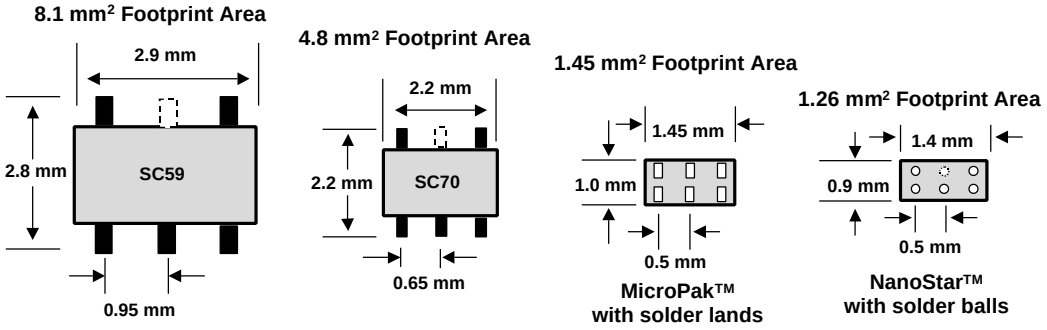

Figure 2. Footprint comparisons of single and dual gate packages

Leaded triple gate packages and some dual gate packages have 8 leads and have lead pitches of 0.5 mm and 0.65 mm as shown in Figure 3.

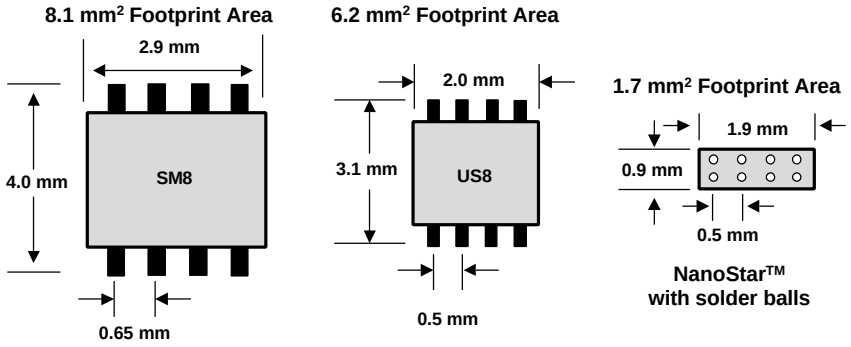

Figure 3. Footprint comparisons of dual and triple gate packages

These smaller logic devices are available in different product families to fit speed or drive requirements of different applications. Note that equivalent product families among vendors can have different naming conventions even though parts have the same technical characteristics. Vendors offering these parts include Philips, Toshiba, TI, Fairchild, ON, IDT, and Pericom. Table 3 shows multiple gate families with their corresponding single, dual, and triple gate families:

Equivalent Multi-Gate Family	Single Gates	Dual Gates	Triple Gates
74LVC, 74LCX	74LVC1G, TC7SZ, NC7SZ, NL17SZ	74LVC2G, NC7WB, NL27WZ	74LVC3G, NC7NZ, NL37WZ
	PI74ST1G, PI74STX1G	PI74STX2G	PI74STX3G
74CBTLV	74CBTLV1G		
74AUC16	74AUC1G, NC7SV	74AUC2G	74AUC3G

Table 3. Low voltage logic single, dual and triple gate families

Mixed Voltage Systems

Legacy 5-volt systems co-exist with newer low voltage systems, and there is a need for the different voltage systems to interface to each other. There are a number of low voltage families that have capability to interface with 5 V devices on the inputs, outputs, or both. Also, 3.3-volt devices need the capability to interface to either 2.5-volt or 1.8-volt devices.

When mixing logic devices from different voltage systems, the I/O pins must be able to tolerate voltages from the higher voltage system. Some CMOS logic families have clamp diodes on the inputs that become forward biased and create a current path to V_{CC} when an overvoltage condition exists. Other CMOS families remove diode paths to V_{CC} thus providing overvoltage tolerance (Figure 4).

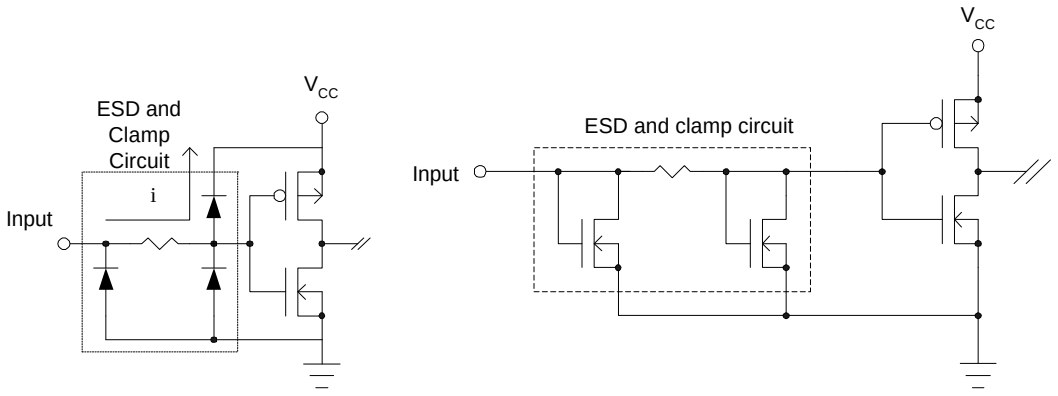

Figure 4. CMOS input circuits with and without V_{CC} clamp diodes

On outputs, circuitry must be able to tolerate an overvoltage condition in the high impedance mode, a logic HIGH state, or both. Many low voltage families have output protection circuitry to allow overvoltage conditions. Table 4 summarizes the operating voltages of various low voltage families and the overvoltage capabilities of their I/Os.

Logic Family	Optimized for 3.3 V	Operates at 3.3 V	Optimized for 2.5 V	Operates at 2.5 V	Optimized for 1.8 V	Operates at 1.8 V or Lower	Overvoltage Tolerant on I/Os
LV	✓					✓	Limited to V_{CC}
LVC, LCX	✓			✓		✓	5 V
ALVC	✓			✓		✓	5 V on non-bus hold inputs
LVT	✓						5V
ALVT	✓			✓			5 V
AVC		✓	✓			✓	3.3 V
AUC				✓	✓	✓	3.3 V
LVX	✓			✓			5 V on inputs
LPT	✓						5 V
VCX		✓	✓			✓	3.3 V

Table 4. Logic Family Operating Voltages

In addition to I/Os tolerating overvoltage conditions, an output must be able to adequately drive a receiver's V_{IH} and V_{IL} levels. A 3 volt driver can easily drive a 5 volt receiver if the input levels are TTL. However, if the input levels are 5 volt CMOS, the 3 V driver's V_{OH} level will not be high enough. Figure 5 shows a comparison of CMOS versus TTL switching standards:

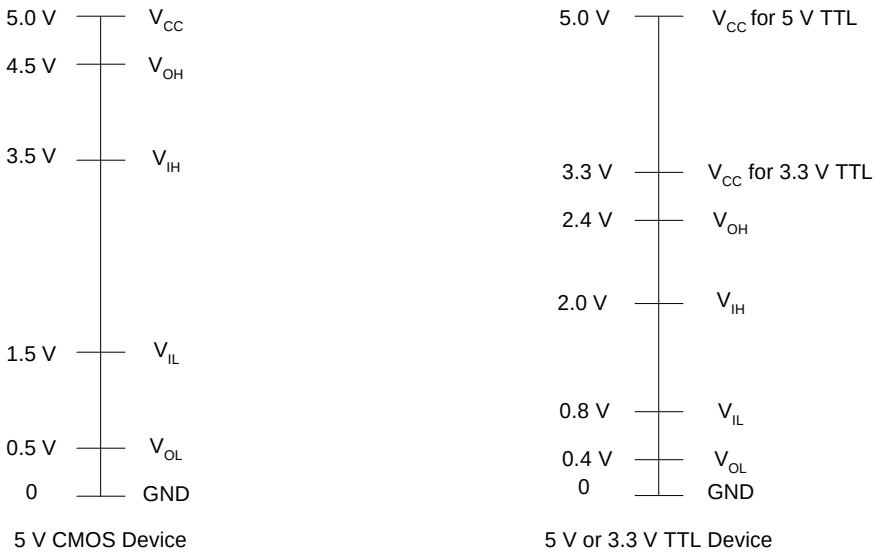

Figure 5. 5 volt CMOS vs. TTL levels

The switching levels for CMOS inputs are 70% of V_{CC} for V_{IH} and 30% of V_{CC} for V_{IL}. A 3-volt driver must reach 3.5 V to meet the V_{IH} level. In this case, a level shifter with dual V_{CC} supplies is needed to ensure a rail-to-rail 5 V signal swing. Figure 6 shows possible solutions using two types level shifters available on the market. These level shifters are offered in the LVX, LVC, LCX, ALVC, AVC, or VCX families: If only a few signals need to be shifted, open-drain devices like the 06 or 07 functions can be used if the family has 5 volt tolerant outputs

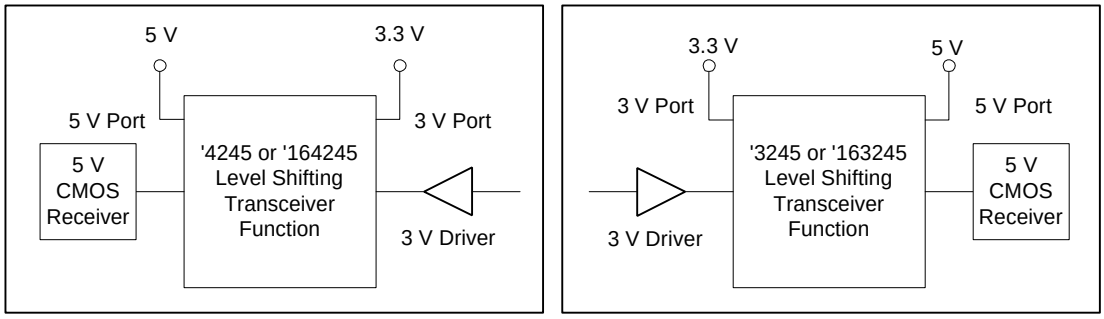

Figure 6. Level shifters to interface between 3 volt and 5 volt systems

Several scenarios exist when mixing and matching mixed voltage devices. Attention must be paid to overvoltage tolerance and meeting input switching levels. Figure 7 shows solutions how to interface among these scenarios for different logic families:

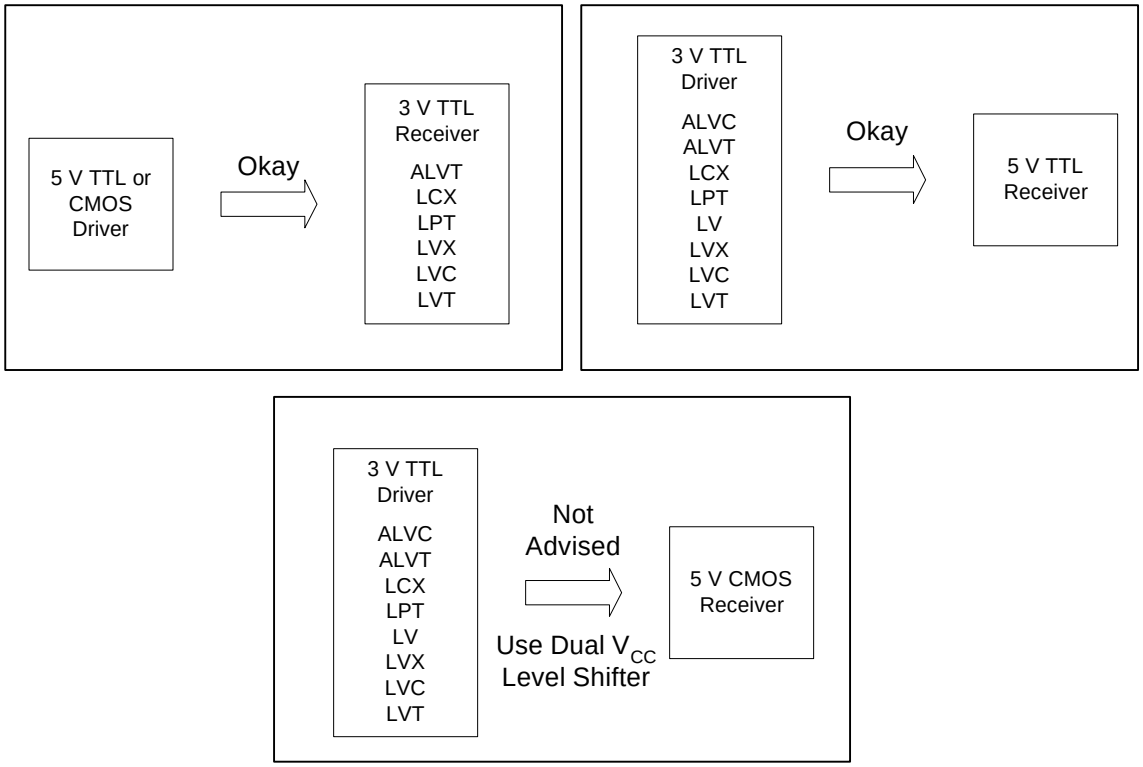

Figure 7. Interface scenarios with 3 volt and 5 volt devices

Hot Swapping

Inserting and removing PC boards without turning off the power is increasingly a requirement for high-availability systems such as telecom equipment, real-time transaction processing, air-traffic control, and fault-tolerant computing. Such systems can have only minimal down time. So the ability to exchange hardware without affecting the system is important. This capability goes by the names of "live insertion," "hot plugging," and "hot swapping." Implementing live insertion requires careful hardware and software design. Various logic and bus-switch families have different capabilities and design considerations when used in live insertion applications.

A key issue during live insertion is maintaining data integrity on the system bus while preventing damage to the components of the host system or those on the live-inserted PC board. Components must meet one of the three levels of bus isolation:

- First level: The construction of the components is such that, when unpowered, they will not be damaged when connected to a live bus. Further, so that a component's input or output pins that are connected to the interface will not load down the system bus, its outputs must remain in a high impedance state and have a “power-off disable” feature and support partial power-down mode. Parts will have an “I_{OFF}“spec in the data sheet if the device has this feature.

- Second level: Hot-swap components support partial power-down mode and include circuitry to keep their outputs high impedance during power-up or power-down. A power-up/power-down 3-state circuit prevents loading and conflicts on a live bus. System software must be able to detect the live-insertion event, detect and correct any bus errors, and re-initialize the bus as needed. An I_{PU}/I_{OZPD} or an I_{OZPU}/I_{OZPD} spec in the data sheet indicates the power-up/power-down feature.

- Third level: The third level of isolation includes the previous two levels and adds circuitry to precharge the bus of the PC board being inserted to a preset voltage level. The precharge voltage helps reduce glitches caused by the bus's impedance and capacitance at the live-insertion interface. Devices with this feature will have a section in the data sheet that has precharge bias voltage and current specs.

Many low voltage logic families support live insertion by providing one of the 3 levels of isolation previously mentioned. Removing diode paths to V_{CC} on inputs and by adding protection and precharge bias circuitry on outputs does this. Table 5 summarizes how different logic families support hot swapping:

Logic Family	Supports Power-off Disable, IOFF	Supports Power-up/down 3-State	Has Pre-charge Bias Circuitry
LVC, LCX, ALVC, VCX	✓		
LVCZ, LCXZ, LVT, ALVT	✓	✓	
FBL, GTLP	✓	✓	✓
CBTLV, PI3C, QS3	NA	NA	✓

Table 5. Low voltage logic families that support hot swapping

Digital Low Voltage Bus Switches

You can't implement every logic function in an ASIC of FPGA. A bus switch function is a good example. The bus switch is designed for the high-speed digital communication systems requirement, where buses need to provide faster connection, bus isolation, and better protection. The low voltage digital bus switch is designed for this type of application. These switches provide low ON resistance connections between device and I/O ports without adding significant propagation delay (typically 0.25 ns). Furthermore, the bus switches feature hot insertion capability and lower power consumption.

Memory Module Application:

The new microprocessor requires faster access time to memory devices. One technique to improve the access time is to distribute the data in several memory banks. You can further improve the memory access time by placing the digital bus switch between memory and the MPU. For example in Figure 8, the MPU first fetches the first 16 bits of data after 25ns and then a few nanoseconds later reads the second word of data via the second channel of the CBTLV multiplexer.

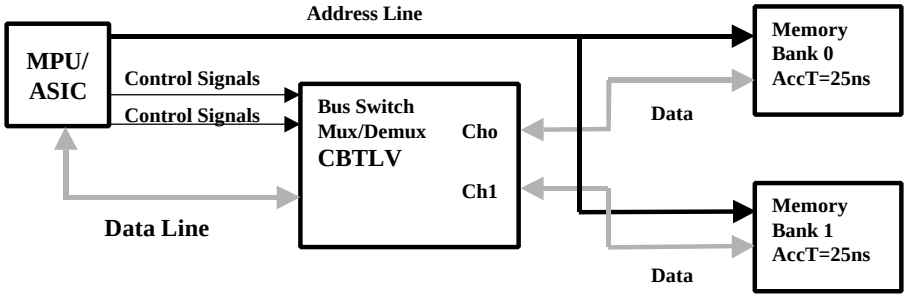

Figure 8. Multiplexing data lines in memory banks

High-end Server Hot Swap Application:

As the companies transfer their critical applications onto servers, the servers are required to support hot insertion in order to minimize downtime.

Hot insertion digital bus switches have pre-charge circuitry and fully support all levels of bus isolation. These devices allow the PC board either to be inserted or removed from the motherboard's slot without the need to power down the server (Figure 9).

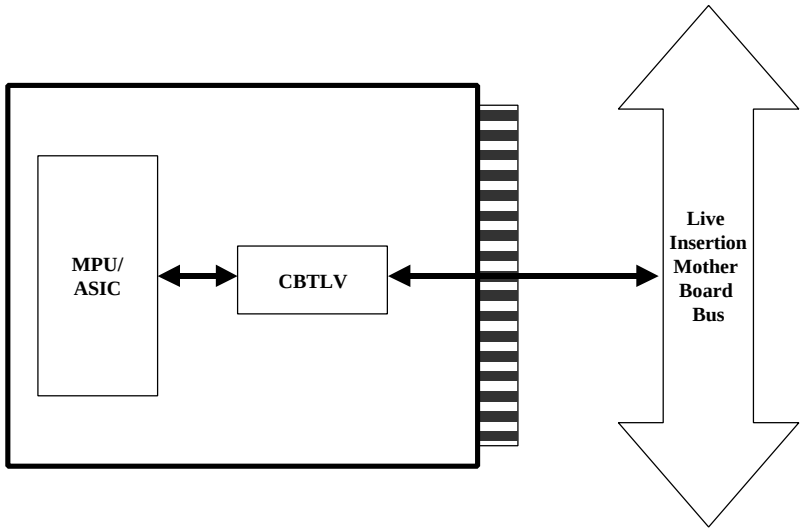

Figure 9. Bus switch used for hot swapping

Conclusion

There are a large variety of standard low voltage families available to serve the needs of many applications that don't require the use of ASICs or FPGAs. Today's logic families run at fast speeds, allow interfacing between mixed voltage systems, support hot swapping, and have many package options to choose from, from standard packaging to tiny single, dual, and triple gates. Logic is alive and well, and semiconductor vendors continue to invest in new technologies and smaller packaging.

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